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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,059	06/29/2001	Debashis Bhattacharya	162.7107USU	9475

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EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/896,059	Applicant(s) BHATTACHARYA ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-19 and 21-61* is/are rejected.

7)☒ Claim(s) *10 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 July 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicants' Amendment to application 09/896,059, has been examined. The drawings are amended. Claims 2-5, 9, 11-20, 22-25 are amended. Claims 31-61 are added. Claims 1-61 are pending.

Drawings

1. Applicants' amended drawings, received on 2 July 2003 are approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 9, 19, 29, 31, 39, 47 and 54** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are between optimization metric and the optimizing and designing steps. Applicants must clarify within the claim language what the optimization metrics are and how they relate to the design objectives and design-specific cell. **Claims 32-38, 40-46, 48-53, and 55-61** are likewise rejected under this code section based on dependency.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Rejection of claims 1, 2, 20, 21 and 30

5. **Claims 1, 2, 20, 21, and 30** are rejected under 35 U.S.C. 102(e) as being anticipated by Gan et al., U.S. Patent 6,308,309. Gan discloses a method of parallel custom block design that permits parallel design.

6. Pursuant to claim 1, [a]n automated method for designing integrated circuits (col. 1 to col. 2, line 27 discloses an automated method of circuit design), comprising steps of describing the IC (col. 2, ll. 29-31), the description including at least one design objective (col. 2, ll. 27-30 disclose design objectives that include area, logic, timing and placement) of said IC; partitioning said description into at least one functional block (col. 4, ll. 12-21 disclose the use of bounding boxes which effectively accomplish partitioning); generating at least one design-specific cell representative of said functional block, said design-specific cell generated based on said design objective of said IC (col. 3, ll. 50-63).

7. Pursuant to claim 2, wherein said step of generating comprises evaluating said design-specific cell based on the context in which said design-specific cell is to be used (col. 3, ll. 57-61; col. 4, ll. 61-67).

8. Pursuant to claims 20 and 30, these claims incorporate the limitations already rejected in claim 1 and the additional limitations of a design specific cell (col. 2, ll. 39-59) and a storage medium having computer readable program instructions (col. 2, ll. 47-52) are additionally disclosed in Gan.

9. Pursuant to claim 21, this claim incorporates the limitations already rejected in claim 2 and likewise rejected here based on the same reasoning.

Rejection of claims 1-8, 11-18, and 21-28

10. **Claims 1-8, 11-18, and 21-28** are rejected under 35 U.S.C. 102(e) as being anticipated by Katsioulas et al. (Katsioulas). Katsioulas discloses a standard block architecture for integrated circuit design.

11. Pursuant to claim 1, [a]n automated method for designing integrated circuits (col. 7, ll. 6-10 discloses an automated method of circuit design), comprising steps of describing the IC (col. 2, ll. 29-31), the description including at least one design objective (col. 5, ll. 38-47) of said IC; partitioning said description into at least one functional block (col. 10, ll. 65-67); generating at least one design-specific cell representative of said functional block, said design-specific cell generated based on said design objective of said IC (the Standard Block, col. 10, line 67 to col. 11, line 8).

12. Pursuant to claim 2, wherein said step of generating comprises evaluating said design-specific cell based on the context in which said design-specific cell is to be used (col. 9, ll. 45-67).

13. Pursuant to claim 3, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set of at least one cell based on said IC design objective (col. 8, ll. 31-35; col. 20, ll. 48-63).

14. Pursuant to claim 4, wherein said step of characterizing and selecting is repeated until the design objective is met (col. 3, ll. 44-62).

15. Pursuant to claim 5, wherein said design objective is selected from a group consisting of : area, performance, power consumption. . . (col. 19, ll. 20-35).

16. Pursuant to claim 6, further comprising a step of optimizing the IC design (col. 2, ll. 45-56).

17. Pursuant to claim 7, wherein a criteria for the step of optimizing is selected from a group consisting of clock speed, transistor sizing. . . (col. 19, ll. 7-34).

18. Pursuant to claim 8, wherein step of optimizing is repeated automatically (col. 2, ll. 45-56).

19. Pursuant to claim 11, this independent claim recites limitations already rejected in claim 1 and the additional claim limitation of a system is disclosed in Katsioulas (col. 7, ll. 6-10, EDA tools).

20. Pursuant to claims 12-18, these claims address limitations already rejected in claims 2-8, respectively, and therefore claims 12-18 are likewise rejected based on the same reasoning.

21. Pursuant to claim 21, this independent claim recites limitations already rejected in claim 1 and the additional claim limitation of a design-specific cell produced by an automated IC design process is disclosed in Katsioulas (col. 7, ll. 23-41, the Standard Block).

22. Pursuant to claims 22-28, these claims address limitations already rejected in claims 2-8, respectively, and therefore claims 22-28 are likewise rejected based on the same reasoning.

Allowable Subject Matter

23. Claims 9, 19, and 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

24. Claims 10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

25. The following is a statement of reasons for the indication of allowable subject matter: In a method for automated design of integrated circuits using dynamically generated building blocks, the prior art does not disclose the generation of a transistor-level design-specific cell.

Remarks

26. Turning first to the Applicants' arguments addressing the rejections under 35 U.S.C. 112, second paragraph, Applicants state that "the cooperative relationship between the claimed IC design objectives and the claimed optimization metric should be clear to one of ordinary skill in the art of the invention." (Amendment, page 13, ¶ 5). It is not. As a matter of fact, the term "optimization metric" is not even disclosed in Applicants' specification. Applicants' specification disclose "conventional metrics" (see, e.g., page 10, line 16) and "design metrics" (see, e.g., page 10, line 18). But the meaning of the term "optimization metric" as it relates to Applicants' invention and the remainder of the claims in which this term is recited, is unclear. Applicants claim an iterative process until "at least one optimization metric" is satisfied. However, nowhere

in the claims has the existence of optimization metrics even been asserted. The probability even exists that Applicants intended to claim some other feature. Nevertheless, the burden of clarification for this unclear and unspecified limitation rests with Applicants and accordingly the new and existing claim rejections under this code section are maintained.

27. Next, Applicants assert that Gan does not teach or contemplate the step of partitioning as disclosed by Applicants and therefore the rejection under 35 U.S.C. 102 is erroneous. In addition to the cite used in the Office Action to support the rejection, Examiner further cites column 4, lines 25-29, which states in part,

> Phantom blocks. . . could also be e.g. a reserved area, an HDL behavioral mode with a reserved area, an HDL structural model with a reserved area, or **fully defined custom blocks**. (emphasis added)

The cells disclosed in Gan may be cells with real functionality, contrary to Applicants' assertion.

28. Additionally, Applicants assert that Katsioulas teaches away from partitioning a description of the IC design into functional blocks. (Amendment, page 16, ¶ 1). But, in addition to the supporting cites provided in the Office Action, Katsioulas clearly discloses at column 10, lines 65-67 which states in pertinent part,

> As explained, STANDARD BLOCKs are created by partitioning IC design (e.g. RTL full hierarchy or netlist) into smaller parts or modules. The partitioning is based, for example, on **functionality**. . .. (emphasis added)

Standard blocks *are* functional blocks of logic; they are not new, independent entities devoid of function and logic.

29. Therefore, based on the foregoing reason, supra, Applicants' claims, original, amended, and newly added, are unpatentable.

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

32. Responses to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Master's Level Patent Examiner

22 September 2003